METHOD AND APPARATUS FOR DECODING IMAGE HAVING FORMAT FOR DIGITAL CAMCORDER

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method and apparatus for decoding an image having a format for a digital video camera so called a digital camcorder (DV), that can minimize the memory capacity required for implementing a variable-length decoder and the operation time for searching blocks when decoding bit streams encoded in a format for the digital camcorder (DV).

Background of the Related Art

[0002] Recently, the use of a digital image has been expanded. Especially, a moving image is generally stored and transmitted after being compressed and encoded since lots of resources are required for storing and transmitting the moving image. As the standard widely used for this purpose, there exist an MPEG (moving picture experts group)-1 and an MPEG-2 based on a discrete cosine transform (DCT) and motion estimation and compensation technique, which are actively applied to a video compact disc (CD), a digital versatile disc (DVD), a digital television, etc. Currently, they are substituted for the existing

analog video reproducing appliances for home use, while a digital camcorder (DV) is substituted for a camcorder that is the existing analog recording and reproducing appliance.

[0003] The digital camcorder requires an encoder having the complicated standard of an MPEG series, and this causes the application of such an encoder to be limited to broadcasting appliances. Also, the digital camcorder is designed to have a different construction from the MPEG considering the characteristics in that both an encoder and a decoder should be included in the camcorder. Especially, since a motion estimation and compensation section generally used in the standard of the MPEG and so on requires a high-order operation amount, it is difficult to mount the motion estimation and compensation section onto a general home appliance. This causes the compression and encoding standard of a simple structure that does not perform the motion estimation and compensation to be proposed.

[0004] This encoding standard for the digital camcorder is disclosed in "IEC 61834-2 Recording - Helical-scan digital video cassette recording system using 6.35mm magnetic tape for consumer use (525-60, 625-50, 1125-60, and 1250-50 systems) - Part 2: SD format for 525-60 and 625-50 systems." This standard is generally called a DV format.

[0005] As the use of the digital camcorder adopting the DV format is spreading, there has been an increasing demand for an

additional function for processing data of the DV format in a home video appliance such as a digital television receiver as well as the function of the digital camcorder itself.

[0006] According to the DV format, the whole image is divided into two types of macro blocks as shown in FIGs. 1 and 2. The 525-60 system uses either of the two types of macro blocks in accordance with the position in the image, while 626-50 system uses only the type of macro blocks in FIG. 2. As is common to the two types of macro blocks, DCT blocks DCT0~DCT5 for four luminance signals Y0, Y1, Y2, and Y3 and two chrominance signals CR and CB are sequentially encoded as shown in FIG. 3. The respective DCT block is a unit block for performing the DCT, and is composed of 8*8 pixels. At this time, in distinction from the compression and encoding standard of the MPEG series, a fixed bit amount is allocated to each video segment in the DV format for the strict management thereof.

[0007] That is, as shown in FIG. 4, one video segment is composed of 5 macro blocks. Thus, 30 DCT blocks constitute one video segment.

[0008] Also, since a trick-mode reproducing function is important according to the characteristic of the camcorder, a DC coefficient of the respective block is written in a fixed position for a high-speed forward/reverse reproduction. At this

time, AC coefficients are sequentially stored in the remaining places except for the place where the DC coefficient is written.

[0009] A general encoding process for storing the AC coefficients is performed as follows.

[0010] (a) The bit stream obtained as a result of compression and encoding of the respective DCT blocks is sequentially written in a basic area allocated in the respective DCT block. The basic area allocates 14 bytes to a luminance-component block, and 10 bytes to a chrominance-component block. At this time, if the bit stream exceeds the allocated basic area, the encoding of the corresponding DCT block is stopped, and the next DCT block is processed.

[0011] (b) The step (a) is performed with respect to 30 DCT blocks.

[0012] (c) The processing of the DCT block stopped at the step (a) in the respective macro block continues. That is, the excess portion of the DCT block that exceeds the basic area at the step (a) is stored in a surplus portion of the basic area allocated to another DCT block whose encoding is completed.

[0013] (d) The step (c) is repeatedly performed with respect to 5 macro blocks until the excess portion or the surplus portion in the respective macro block vanishes completely. As a result, one part of the 5 macro blocks which constitute the video segment

has the surplus portion, and the other part has the excess portion.

[0014] (e) The excess portion of the macro block that exceeds the basic area is stored in the surplus portion of the basic area allocated to another macro block. Here, the basic area allocated to the macro block means the sum of basic areas allocated to the DCT blocks included in the respective macro block.

[0015] (f) The step (e) is repeatedly performed with respect to the whole region of the video segment until the excess portion or the surplus portion vanishes completely.

[0016] The decoding of the bit streams encoded as described above is generally performed according to the following order.

[0017] (a) The variable-length decoding is sequentially performed with respect to the DCT blocks in the respective macro block. The decoded data is sequentially stored in a storage device. At this time, if an end of block (EOB) of the DCT block is not transmitted at a time point when all the data of the basic area allocated to the corresponding DCT block is decoded, the decoding of the corresponding DCT block is stopped, and the next DCT block is decoded.

[0018] (b) The step (a) is performed with respect to 30 DCT blocks.

[0019] (c) The decoding of the DCT block in the macro block, of which the EOB is not transmitted, i.e., the DCT block that is

judged to exceed the basic area allocated at the step (a), continues through the readout of the bit stream from the surplus portion of the basic area allocated to the DCT block of which the EOB is transmitted, i.e., the DCT block whose decoding is completed.

[0020] (d) The step (c) is continuously performed until the surplus portion or the excess portion in the macro block vanishes completely.

[0021] (e) The decoding of the 6 DCT blocks in the macro block whose decoding is not completed continues through the readout of the bit stream from the surplus portion of the basic area allocated to the macro block in which the decoding of the 6 DCT blocks is completed.

[0022] (f) The step (e) is repeatedly performed until the decoding of all the macro blocks is completed. In a normal condition, the completion of decoding of the video segment means that the EOBs of the 30 DCT blocks are detected.

[0023] Conventionally, the complicated process as described above is performed for the decoding of the video segment, and this causes the design of the storage device and control logic circuit to exert an important effect upon the cost and performance of the system.

[0024] Specifically, since the decoding process is performed in the unit of a video segment, a storage device for storing a

bit stream for one video segment is basically required, and its size should be of (14*4+10*2)*8*5 = 3,040 bits as defined in the standard. In practice, a double buffer is used for the real-time process, and thus two storage devices are necessary.

[0025] The capacity of the storage device required for the following process is determined according to the implementation method of the variable-length decoder. At this time, in case of implementing the variable-length decoder according to the above method, a storage device for storing DCT coefficients for two video segments, i.e., 60 DCT blocks, is required for the real-time process since an inverse DCT (IDCT) can be performed after the variable-length decoding is completed in all.

[0026] Since 64 DCT coefficients are included in one DCT block, the capacity of the storage device will be of 30,720 bits. Also, since the decoding process should be repeatedly performed in the unit of a DCT block, a macro block, and a video segment, a temporary storage device for storing the bit stream obtained as a result of performing the respective steps also requires the size of one video segment, which is the same size as the storage device for storing the input bit stream, i.e., 3,080 bits.

[0027] Also, in case of the DCT block that exceeds the allocated basic area, the bit stream of another DCT block whose decoding is completed should be searched in order to read out its

own bit stream stored in the surplus space of another DCT block. This requires a long operation time.

SUMMARY OF THE INVENTION

[0028] Accordingly, the present invention is directed to a method and apparatus for decoding an image of a DV format that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0029] An object of the present invention is to provide a method and apparatus for decoding an image of a DV format that can perform the variable-length decoding and the IDCT within a given time by judging whether respective DCT blocks can be decoded to a bit stream allocated with a fixed size at the front end of the variable-length decoder and preferentially decoding the DCT blocks judged to be able to be decoded.

[0030] Another object of the present invention is to provide a method and apparatus for decoding an image of a DV format that removes the necessity of a separate storage device for temporarily storing a result of decoding in a basic area in case that the EOB of a DCT block is positioned outside the basic area by redefining the processing order of the blocks.

[0031] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary

skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0032] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of decoding an image of a DV (digital camcorder) format includes a preprocessing step of detecting a position of an EOB (end of block) of a respective DCT (discrete cosine transform) block using length information of a variable-length code of a bit stream encoded in the DV format, and a step of redefining a processing order of the DCT blocks according to the position of the EOB detected at the preprocessing step, and performing a variable-length decoding with respect to the respective DCT blocks in the redefined processing order.

[0033] Preferably, the variable-length decoding step performs the variable-length decoding in the order of all complete DCT blocks in complete macro blocks, all incomplete DCT blocks in complete macro blocks, all complete DCT blocks in incomplete macro blocks, and all incomplete DCT blocks in incomplete macro blocks in a corresponding video segment in accordance with

contents of a DCT block index vector and a macro block index vector.

[0034] In another aspect of the present invention, an apparatus for decoding an image of a DV (digital camcorder) format includes a preprocessor for detecting a position of an EOB (end of block) of respective DCT (discrete cosine transform) blocks using length information of a variable-length code of a bit stream encoded in the DV format, a variable-length decoding section for redefining a processing order of the DCT blocks according to the position of the EOB detected by the preprocessor, and performing a variable-length decoding with respect to the respective DCT blocks in the redefined processing order, a storage device for receiving and outputting to the preprocessor the encoded bit stream, and storing and outputting the EOB of the respective DCT blocks outputted from the preprocessor and DCT coefficients variable-length-decoded by the variable-length decoding section, and a control section having built-in DCT block index vectors, macro block index vectors, and a bit address register to redefine a variable-length decoding order of the variable-length decoding section, and outputting to the storage device the number of the respective DCT blocks to be processed, a read signal, and a write signal in accordance with values of the DCT block index vectors.

[0035] Preferably, the preprocessor prepares a simple code table according to a length stored in a variable-length code table of the variable-length decoding section, and performs a pseudo-variable-length decoding accordingly.

[0036] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0038] FIG. 1 is a view illustrating an example of the process of dividing the whole image of a general DV format into macro blocks;

[0039] FIG. 2 is a view illustrating another example of the process of dividing the whole image of a general DV format into macro blocks;

[0040] FIG. 3 is a view illustrating an example of the macro block of FIGs. 1 and 2 that is composed of DCT blocks DCT0~DCT5 for four luminance signals and two chrominance signals;

[0041] FIG. 4 is a view illustrating an example of a general video segment composed of 5 macro blocks MB0~MB4;

[0042] FIG. 5 is a view illustrating a DCT block index vector, CDB counter, EOB counter, address register 0, address register 1, and address register 2 used for separating and rearranging complete DCT blocks and incomplete DCT blocks according to the present invention;

[0043] FIG. 6 is a view illustrating a DCT block index vector, CMB counter, address register 1, and address register 2 used for separating and rearranging complete macro blocks and incomplete macro blocks according to the present invention;

[0044] FIG. 7 is a view illustrating a bit address register used for storing bit addresses whose variable-length decoding is stopped according to the present invention;

[0045] FIG. 8A is a view illustrating a complete/incomplete DCT block judgment result of 6 DCT blocks in a macro block of FIG. 3 according to the present invention;

[0046] FIG. 8B is a view illustrating an example of a DCT block index vector prepared on the basis of FIG. 8A;

[0047] FIG. 9 is a block diagram of an apparatus for variable-length decoding an image of a DV format according to the present invention;

[0048] FIG. 10 is a detailed block diagram of a preprocessing section in FIG. 9; and

[0049] FIG. 11 is a detailed block diagram of a variable-length decoding section in FIG. 9.

DETAILED DESCRIPTION OF THE INVENTION

[0050] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0051] In the present invention, among DCT blocks DCT0~DCT5, a basic area of 14 bytes is allocated to four luminance components for the DCT blocks DCT0~DCT3, and a basic area of 10 bytes is allocated to two chrominance components for the DCT blocks DCT4 and DCT5, respectively.

[0052] For convenience' sake in explanation, the DCT block whose end of block (EOB) is produced within the above range, i.e., the DCT block whose decoding is completed, is called a 'complete DCT block', and the contrary DCT block is called an 'incomplete DCT block'.

[0053] Meanwhile, a basic area of 14*4+10*2 = 76 bytes is allocated to macro blocks MB0~MB4, respectively.

[0054] Also, for convenience' sake in explanation, the macro block where all the EOBs of 6 DCT blocks are produced within the above range, i.e., the macro block whose decoding is completed, is called a 'complete macro block', and the contrary macro block is called an 'incomplete macro block'. Since even the EOB of an incomplete DCT block may be produced from a surplus bit stream of the basic area allocated to a different complete DCT block, the complete macro block is not always composed of 6 complete DCT blocks.

[0055] Meanwhile, in order to separate and rearrange the complete DCT blocks and the incomplete DCT blocks, DCT block index vectors as shown in FIG. 5 are used. Specifically, 5 DCT block index vectors are used for each macro block, and the respective size, i.e., the number of elements in the vector, corresponds to the number of DCT blocks in the macro block, i.e., 6. The DCT block number is written in the respective element.

[0056] An address register 0 has the number of the first complete DCT block having a surplus bit stream, and is used for initializing an address register 1. Also, the initial value of the address register 0 is 0. The address register 1 and address register 2 have values in the range of 0 to 5 that indicate the elements of the DCT block index vector. The initial value of the address register 2 is 5. That is, in the initial state, the address register 1 and the address register 2 have 0 and 5,

respectively, and thereafter, the result of initialization of the address register 1 may be a different value according to the value of the address register 0. Also, a complete DCT block (CDB) counter and an end of block (EOB) counter have the number of complete DCT blocks in the macro block and the number of EOBs, respectively, and their initial values are all 0. The complete DCT block always includes the EOB. However, since the EOB of the incomplete DCT block may be produced from the surplus bit stream of the basic area allocated to a different complete DCT block, the value of the EOB counter is always the same as or larger than the value of the CDB counter.

[0057] Also, in order to separate and rearrange the complete macro blocks and the incomplete macro blocks, a macro block index vector as shown in FIG. 6 is used. At this time, since the number of macro blocks in the video segment is 5, the size of the macro block index vector, i.e., the number of elements in the vector, is also 5. An address register 1 and an address register 2 have values in the range of 0 to 4 that indicate elements of the macro block index vector, and their initial values are 0 and 4, respectively. A complete macro block (CMB) counter has the number of complete macro blocks in the video segment, and its initial value is o.

[0058] Also, in order to store bit addresses where the variable-length decoding is stopped, bit address registers as

shown in FIG. 7 are used. The bit address register is allocated to each DCT block, and thus 30 bit address registers are used for one video segment. In case of the incomplete DCT block, the bit address register stores the position where the variable-length decoding is stopped, i.e., the position where the decoding is resumed during the next decoding process, while in case that the EOB is detected, it stores the next bit address, i.e., the start position of the surplus bit stream.

[0059] The method of decoding an image signal of a DV format as constructed above according to the present invention includes a preprocessing (pseudo-variable-length decoding) step and a variable-length decoding step.

[0060] Hereinafter, the preprocessing step and the variable-length decoding step will be explained in order.

[0061] 1. The preprocessing (i.e., pseudo-variable-length decoding) step

[0062] The decoding at the preprocessing step means that the decoding is not actually performed, but the position of the EOB of the respective DCT block is detected using length information of the variable-length code.

[0063] (a) Values of the DCT address register 1, address register 2, CDB counter, and EOB counter of all the DCT block index vectors, and values of the MB address register 1, address

register 2, and CMB counter of the macro block index vector are initialized.

[0064] (b) If the DCT block is the complete DCT block, the position of the bit following the EOB is written in the bit address register of FIG. 7. Then, the corresponding DCT block number is written in the element of the DCT block index vector of FIG. 5 that is indicated by the address register 1, and then the value of the address register 1 is increased. If the DCT block is the incomplete DCT block, the position where the decoding is stopped is written in the bit address register of FIG. 7. Then, the corresponding DCT block number is written in the element of the DCT block index vector of FIG. 5 that is indicated by the address register 2, and then the value of the address register 2 is decreased.

[0065] (c) The step (a) is sequentially performed with respect to 6 DCT blocks in the macro block. FIGs. 8A and 8B exemplify this process. That is, FIG. 8A shows a result of complete/incomplete DCT judgment of 6 DCT blocks in a macro block as shown in FIG. 3, and FIG. 8B shows DCT block index vectors prepared based on this result of judgment.

[0066] (d) If the value of the CDB counter is smaller than 6, the values of the DCT address register 1 and the address register 2 are reinitialized, and the processing of the incomplete DCT blocks is resumed. At this time, the address register 2 has the

address of the vector element that has the number of the incomplete DCT block to be processed, and the address register 1 has the address of the vector element that has the number of the complete DCT block from which the bit stream to be used for decoding the incomplete DCT block is read out. Also, the bit position in which the decoding of the incomplete DCT block is to be resumed is read out from the bit address register of the incomplete DCT block, and the position in which the bit stream is to be read out from the complete DCT block is read out from the bit address register of the complete DCT block. In other words, the decoding is resumed in the position indicated by the bit address register of the incomplete DCT block, and over the basic area, the bits are subsequently read out in the position indicated by the bit address register of the complete DCT block.

[0067] (e) If the EOB is detected during performing the step (d), the value of the EOB counter is increased. Thereafter, if the increased value of the EOB counter is smaller than 6, the value of the address register 2 is decreased, and then a new incomplete DCT block is selected with reference to the element indicated by the value of the address register 2. Then, the decoding of the incomplete DCT block continues. If the increased value of the EOB counter becomes 6, it means that the present macro block is the complete macro block. In this case, the number of the present macro block is written in the element indicated by

the MB address register 1 of FIG. 6, and the value of the address register 1 and the value of the CMB counter are increased in order.

[0068] (f) If the surplus bit stream of the basic area allocated to the complete DCT block vanishes completely during performing the step (d), the value of the DCT address register 1 is increased. Thereafter, if the increased value is smaller than the value of the CDB counter, a new complete DCT block is selected with reference to the element indicated by the value of the DCT address register 1, and the decoding continues using the surplus bit stream of the basic area allocated thereto. If the increased value of the DCT address register 1 is the same as the value of the CDB counter, it means that the present macro block is the incomplete macro block. In this case, the number of the present macro block is written in the element indicated by the MB address register 2 of FIG. 6, and the value of the address register 2 is decreased.

[0069] (g) The above steps (b)~(f) are performed with respect to the next macro block.

[0070] 2. Variable-length decoding step

[0071] The decoding at the variable-length decoding step means that the variable-length decoding is actually performed. but the position of the EOB of the respective DCT block is detected using length information of the variable-length code. At

this time, the order of decoding is determined according to the contents of the macro block index vector and the DCT block index vector constructed at the step 1 instead of the general sequential process. The element indicated by the MB address register 1 of the macro block index vector constructed at the step 1 has the number of the complete macro block, and the element indicated by the DCT address register 1 of the DCT block index vector corresponding to the macro block has the number of the complete DCT block. In case of preferentially processing the DCT block, the variable-length decoding is possible without any waiting time for searching the EOB outside the basic area. Thus, only a DCT-counting storage device for one DCT block is required instead of a DCT-counting storage device for the whole video segment, i.e., 30 DCT blocks.

[0072] (a) The DCT address register 0, address register 1, and address register 2, and EOB counter of all DCT block index vectors, and the address register 1 and address register 2 of the macro block index vector are initialized.

[0073] (b) If a completed DCT block is processed, the value of the EOB counter is increased, the value of the address register 1 of the DCT block index vector is increased, and a new complete DCT block determined by this value is processed.

[0074] (c) The step (b) is repeated until the value of the address register 1 coincides with the value of the CDB counter.

[0075] (d) If the step (c) is performed, the value of the address register 1 is initialized, and the incomplete DCT block is processed by the value of the address register 2. At this time, the bit stream is read out with reference to the value of the bit address register of the incomplete DCT block to be processed, and if the bit stream of the basic area vanishes completely, the bit stream is subsequently read out from the position.

[0076] (e) If the bit stream of the basic area allocated to the complete DCT block vanishes completely, the values of the address register 0 and the address register 1 are increased, and the next complete DCT block is selected by the value of a new address register 1.

[0077] (f) If an incomplete DCT block is processed, i.e., if the EOB is detected, the value of the EOB counter is increased, the value of the address register 2 is decreased, and a new incomplete DCT block determined by this value is finished.

[0078] (g) The above steps (d)~(f) are performed until the value of the EOB counter becomes 6, i.e., until the process of the present complete macro block is completed. If the above steps are completed, the position of the next bit where the final EOB is found is written in the bit address register of the present complete DCT block.

[0079] (h) If the process of a complete macro block is completed through the step (g), the value of the address register

1 of the macro block index vector is increased, and if the value is smaller than the value of the CMB counter, the complete macro block corresponding to the number of the macro block of the element indicated by the value of the address register 1 is processed.

[0080] (i) The above steps (b)~(h) are repeated until the value of the address register 1 of the macro block index vector coincides with the value of the CMB counter, i.e., until all the process of the complete macro block is completed.

[0081] (j) If the step (i) is performed, the address register 1 of the macro block index vector is initialized. Then, the value of the address register 1 of every DCT block index vector is initialized. At this time, the address register 0 used for the initialization may have a value that is not 0 through the step (e).

[0082] (k) The incomplete macro block that corresponds to the number of the macro block of the element indicated by the value of the address register 2 is processed. In processing the respective incomplete macro blocks, the complete DCT blocks are preferentially processed through the same method as the steps (b) and (c).

[0083] (l) The incomplete DCT blocks are processed in the same method as the steps (d)~(f).

[0084] (m) If the value of the address register 1 of the DCT block index vector is the same as the value of the CDB counter, the value of the address register 1 of the macro block index vector is increased. Then, if the increased value is smaller than the value of the CMB counter, a new complete macro block is selected, and a new complete DCT block is selected with reference to the value of the address register 1 of the DCT block index vector allocated to the new complete macro block to continue the decoding.

[0085] (n) If the value of the EOB counter is 6, the value of the address register 2 of the macro block index vector is decreased, and the next macro block is selected and processed by the decreased value.

[0086] (o) The above steps (k)~(n) are repeated until the value of the address register 1 of the macro block index vector coincides with the value of the CMB counter.

[0087] According to the variable-length decoding process as described above, the DCT blocks of which the variable-length decoding is possible are preferentially processed according to the order written in the DCT block index vectors, and thus it is not necessary to wait for until another DCT block is processed, with the presently decoded DCT coefficients being stored temporarily.

[0088] FIG. 9 is a block diagram of the DV-format image decoding apparatus for implementing the above-described process by hardware according to the present invention. The decoding apparatus includes a storage device 101, a preprocessing section 102, a control section, and a variable-length decoding section 104.

[0089] The preprocessing section 102 is a pseudo-variable-length decoder, and includes 16-bit registers 201 and 202 and a barrel shifter 203 which are connected at the front end of a pseudo-variable-length decoding section 204 as shown in FIG. 10. The pseudo-variable-length decoding section 204 only provides whether the EOB is transmitted with respect to the inputted bit stream, and the length of the presently inputted variable-length code. At this time, in order to implement the simple preprocessing section 102, a simple code table may be prepared in accordance with the length stored in a variable-length code table.

[0090] In the control section 103 are built the DCT block index vector of FIG. 5, the macro block index vector of FIG. 6, and the bit address register of FIG. 7. The control section 103 outputs the number of the DCT block to be processed according to the value of the DCT block index vector, read and write signals. At this time, the processing order of DCT blocks that corresponds to the contents of the DCT block index vector is in the order of a complete DCT block in a complete macro block, an incomplete DCT

block in a complete macro block, a complete DCT block in an incomplete macro block, and an incomplete DCT block in an incomplete macro block in the corresponding video segment.

[0091] The variable-length decoding section 104 may comprise the general variable-length decoder of FIG. 11 as it is.

[0092] As described above, according to the method and apparatus for decoding an image of a DV format according to the present invention, the blocks that can be processed are preferentially transmitted according to the detection of the EOB in transmitting the bit stream to the variable-length decoder by performing the preprocessing step that is the pseudo-variable-length decoding process with respect to the input bit stream when performing the decoding of the compressed image of the DV format. Thus, the delay that may be produced when the whole block is sequentially processed can be minimized.

[0093] Also, the present invention performs the decoding by redefining the processing order of the DCT blocks, and thus requires a storage device only for one DCT block in comparison to the conventional decoding method that requires a storage device for one video segment, i.e., 30 DCT blocks, in order to store data until DCT coefficients of all the DCT blocks in the video segment are obtained.

[0094] The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The

present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.